ABSTRACT OF THE DISCLOSURE

The present invention discloses a method and system for computer-aided circuit design for checking the equivalence of data flow graphs by splitting data flow graphs representing finite precision arithmetic circuits into lossless subgraphs representing infinite-precision arithmetic circuits, and edges with information loss. The set of lossless subgraphs generated are leveled, and checked for equivalence as expressions. The edges with information loss are compared by establishing the equivalence of their bit width. The present invention declares data flow graphs as equal, if the respective lossless subgraphs and the bit-width at the corresponding edges with information loss are equal.